1. An apparatus comprising:

(1) a difference amplifier comprising:

(a) a first differential pair of terminals for carrying a first differential signal,

(b) a second differential pair of terminals for carrying a second differential signal, and

(c) a third differential pair of terminals for carrying a third differential signal, wherein said third differential signal is based on the difference between said first differential signal and said second differential signal; and

(2) an envelope detector comprising:

(a) a fourth differential pair of terminals electrically connected to said third differential pair of terminals, and

(b) a fifth differential pair of terminals for carrying a fourth differential signal, wherein said fourth differential signal is based on the peak-to-peak amplitude of said third differential signal.

2. The apparatus of claim 1 further comprising:

(3) a low pass filter comprising:

(a) a sixth differential pair of terminals that are electrically connected to said fifth differential pair of terminals, and

(b) a seventh differential pair of terminals for carrying a fifth differential signal.

3. The apparatus of claim 2 wherein said fifth differential signal is a DC signal that is based on the phase difference between said first differential signal and said second differential signal.

4. The apparatus of claim 3 further comprising:

(4) a voltage-controlled oscillator comprising:

(a) an eighth differential pair of terminals that are electrically connected to said seventh differential pair of terminals, and

(b) a ninth differential pair of terminals that are electrically connected to said second differential pair of terminals.

5. An apparatus comprising:

(1) a difference amplifier comprising:

(a) a first terminal for carrying a first signal,

(b) a second terminal for carrying a second signal, and

(c) a third terminal for carrying a third signal, wherein said third signal is based on the difference between said first signal and said second signal; and

(2) an envelope detector comprising:

(a) a fourth terminal electrically connected to said third terminal, and

(b) a fifth terminal for carrying a fourth signal, wherein said fourth signal is based on the peak-to-peak amplitude of said third signal.

6. The apparatus of claim 5 further comprising:

(3) a low pass filter comprising:

(a) a sixth terminal that is electrically connected to said fifth terminal, and

(b) a seventh terminal for carrying a fifth signal.

7. The apparatus of claim 6 wherein said fifth signal is a DC signal that is based on the phase difference between said first signal and said second signal.

8. The apparatus of claim 7 further comprising:

(4) a voltage-controlled oscillator comprising:

(a) an eighth terminal that is electrically connected to said seventh terminal, and

(b) a ninth terminal that is electrically connected to said second terminal.

9. An apparatus comprising:

a first NMOS transistor having a gate terminal, a drain terminal, and a source terminal;

a second NMOS transistor having a gate terminal, a drain terminal, and a source terminal, wherein said drain terminal of said first NMOS transistor is electrically connected to said drain terminal of said second NMOS transistor;

a first resistor having a first terminal and a second terminal, wherein said first terminal is electrically connected to said drain terminal of said first NMOS transistor; and

an envelope detector having a first input terminal, a second input terminal, and a first differential pair of terminals, wherein said first input terminal of said envelope detector is electrically connected to said drain terminal of said first NMOS transistor.

10. The apparatus of claim 9 further comprising:

a third NMOS transistor having a gate terminal, a drain terminal, and a source terminal, wherein said source terminal of said third NMOS transistor is electrically connected to said source terminal of said first NMOS transistor;

a fourth NMOS transistor having a gate terminal, a drain terminal, and a source terminal, wherein said source terminal of said fourth NMOS transistor is electrically connected to said source terminal of said third NMOS transistor, and wherein said drain terminal of said fourth NMOS transistor is electrically connected to said drain terminal of said third NMOS transistor;

a second resistor having a first and second terminal, wherein said first terminal of said second resistor is electrically connected to said drain terminal of said four NMOS transistor, and wherein said second terminal of said second resistor is electrically connected to said second terminal of said first resistor, and wherein said first terminal of said second resistor is electrically connected to said second input terminal of said envelope detector.

11. The apparatus of claim 10 further comprising a fifth NMOS transistor having a gate terminal, a drain terminal, and a source terminal, wherein said drain terminal of said fifth NMOS transistor is electrically connected to said source terminal of said first NMOS transistor.

12. The apparatus of claim 11 wherein said envelope detector measures the peak-to-peak signal of the difference in voltage on said first terminal of said first resistor and said first terminal of said second resistor.

13. The apparatus of claim 11 further comprising a low pass filter comprising:

(a) a second differential pair of terminals, and

(b) a third differential pair of terminals,

wherein said second differential pair of is electrically connected to said first differential pair of terminals.

14. The apparatus of claim 13 further comprising a voltage-controlled oscillator comprising:

(a) a fourth pair of differential terminals,

(b) a first output terminal, and

(c) a second output terminal,

wherein said fourth pair of differential terminals is electrically connected to said third differential pair of terminals, and wherein said first output terminal of said voltage-controlled oscillator is electrically connected to said gate terminal of said second NMOS

transistor, and wherein said second output terminal of said voltage-controlled oscillator is electrically connected to said gate terminal of said fourth NMOS transistor.

15. The apparatus of claim 14 further comprising:

a first input terminal wherein said first input terminal is electrically connected to said gate terminal of said first NMOS transistor;

a second input terminal wherein said second input terminal is electrically connected to said gate terminal of said third NMOS transistor;

a bias input terminal wherein said bias input terminal is electrically connected to said gate terminal of said fifth NMOS transistor;

16. The apparatus of claim 14 further comprising a DC power supply having a positive terminal and a negative terminal, wherein said positive terminal of said power supply is electrically connected to said second terminal of said first resistor, and wherein said negative terminal of said power supply is electrically connected to said source terminal of said fifth NMOS transistor.

17. An method comprising:

comparing a first voltage to a second voltage, wherein comparing said first voltage to said second voltage produces a third voltage that is the difference between said first voltage and said second voltage;

obtaining the peak-to-peak voltage of said third voltage; and

filtering said peak-to-peak voltage wherein a DC voltage is obtained that is based on the phase difference between said first voltage and said second voltage.

18. The method of claim 17 further comprising producing an AC voltage whose frequency is proportional to said DC voltage.

19. The method of claim 18 wherein said first voltage, said second voltage, said third voltage, said peak-to-peak voltage, and said DC voltage are selected from the group consisting of differential and single-ended.

20. An method comprising:

comparing a first current to a second current, wherein comparing said first current to said second current produces a third current that is the difference between said first current and said second current;

obtaining the peak-to-peak current of said third current; and

filtering said peak-to-peak current wherein a DC current is obtained that is based on the phase difference between said first current and said second current.